

### *IN THE SPECIFICATION*

Please replace the paragraph beginning at page 3, line 8, with the following paragraph:

When one of the input ports 28 receives one or more packets, that input port 28 makes a request over control bus 18 to scheduler 26 to send the packets over a back plane cross switch 24 to a particular one of the output ports 29. The scheduler 26 includes arbiters 20 for each output port 20. Separate output port arbitrations are conducted for each output port 29 by a different arbiter 20. The arbiters 20 each conduct an output port arbitration for all of the input ports 28 requesting the same output port 29. The scheduler 26 sends back a grant signal over control bus 18 to the particular input port ~~29~~ 28 winning the output port arbitration.

Please replace the paragraph beginning at page 4, line 17, with the following paragraph:

The VOQ's ~~42~~ 22 prevent Head-of-Line blocking. The VOQs contain a linked list of memory addresses for packets having addresses directed to an associated one of the output ports. The VOQ's can independently request connections to their associated output ports and can ~~be~~ independently be granted a connection request from their dedicated output ports. Thus, packets coming into one of the input ports and directed to a first output port will not block requests from packets coming into that same input port but directed to a different VOQ output port. This means that low priority packets will not block connections requests from other higher priority packets.

Please replace the paragraph beginning at page 7, line 21, with the following paragraph:

With one ~~arbitraiten~~ arbitration iteration, and under heavy load, VOQs with a common output all have the same throughput if all priority and weight are the same. For the matching algorithm that consists of more than one iteration, and under heavy load, VOQs with the same output port may each have a different throughput if all priority and weight are the same.